Description

WF306TBM is one ASK transmitter for remote control application. The circuit working frequency range is about 300MHz-450MHz. It is mainly intended for the ISM (Industrial, Scientific and Medical) band 315/433MHz.

WF306TBM integrates one phase-locked loop (PLL) and MCU to set different working frequency and select the transmitting power.

WF306TBM is designed for remote wireless control systems. It is available in SOP-16 package and working over the extended temperature range (-40 to +85°C).

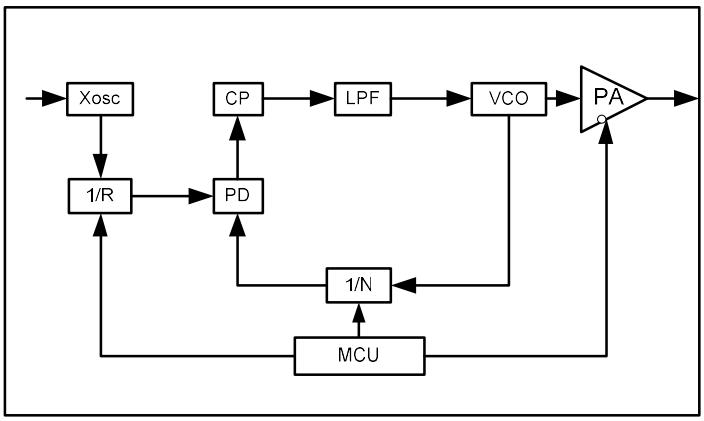
Features

- Working frequency range：300MHz-450MHz.
- Tunable output power : 13dBm @ 3V with 50 ohm load, typ.
- Low supply voltage: 2.3V-3.6V for 315/433MHz.
- Low supply voltage detection
- Automatic shutdown protection
- 3-wire SPI interface.

Applications

- Remote Keyless Entry (RKE)
- Remote Control, Garage door and gate openers
- AMR-Automatic Meter Reading
- Wireless alarm and security system.

Block Diagram



Pin Configuration

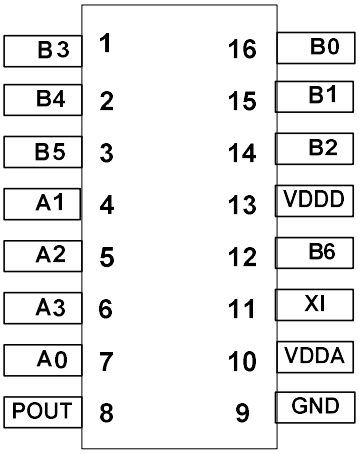


Table 1. Pin Description

Pin	Symbol	I/O	Description
1	B3	I	Input pin or open-drain output pin with system wake-up function System clear (RESET) input. Active low RESET to the device. Weak pull-high always on if configured as RSTB. Voltage on this pin must not exceed VDD, See IOB3 diagram for detail description.
2	B4	I/O	Bi-direction I/O pin with system wake-up function (RCOUT optional in IRC/ERIC, ERC mode) Software controlled pull-high/open-drain Oscillator crystal output (HF, XT, LF mode) Outputs with the instruction cycle rate (RCOUT optional in IRC/ERIC, ERC mode)
3	B5	I/O	Bi-direction I/O pin with system wake-up function(IRC mode) Software controlled pull-high/open-drain Oscillator crystal input(HF,XT,LF mode) Extemal clock source input(ERIC,ERC mode)
4	A1	I/O	A0 ~ A3 as bi-direction I/O pin Software controlled pull-down
5	A2	I/O	A0 ~ A3 as bi-direction I/O pin Software controlled pull-down
6	A3	I/O	A0 ~ A3 as bi-direction I/O pin Software controlled pull-down
7	A0	I/O	A0 ~ A3 as bi-direction I/O pin Software controlled pull-down
8	POUT		Transmitted RF output
9	GND		Ground
10	VDDA		Analog circuit Power suplly
11	XI		Input terminal of local oscillation signal.It is connected to the crystal or driven by an external clock.
12	B6	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain

13	VDDD		Digital circuit Power supply
14	B2	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down External clock input to Timer0
15	B1	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down
16	B0	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down External interrupt input

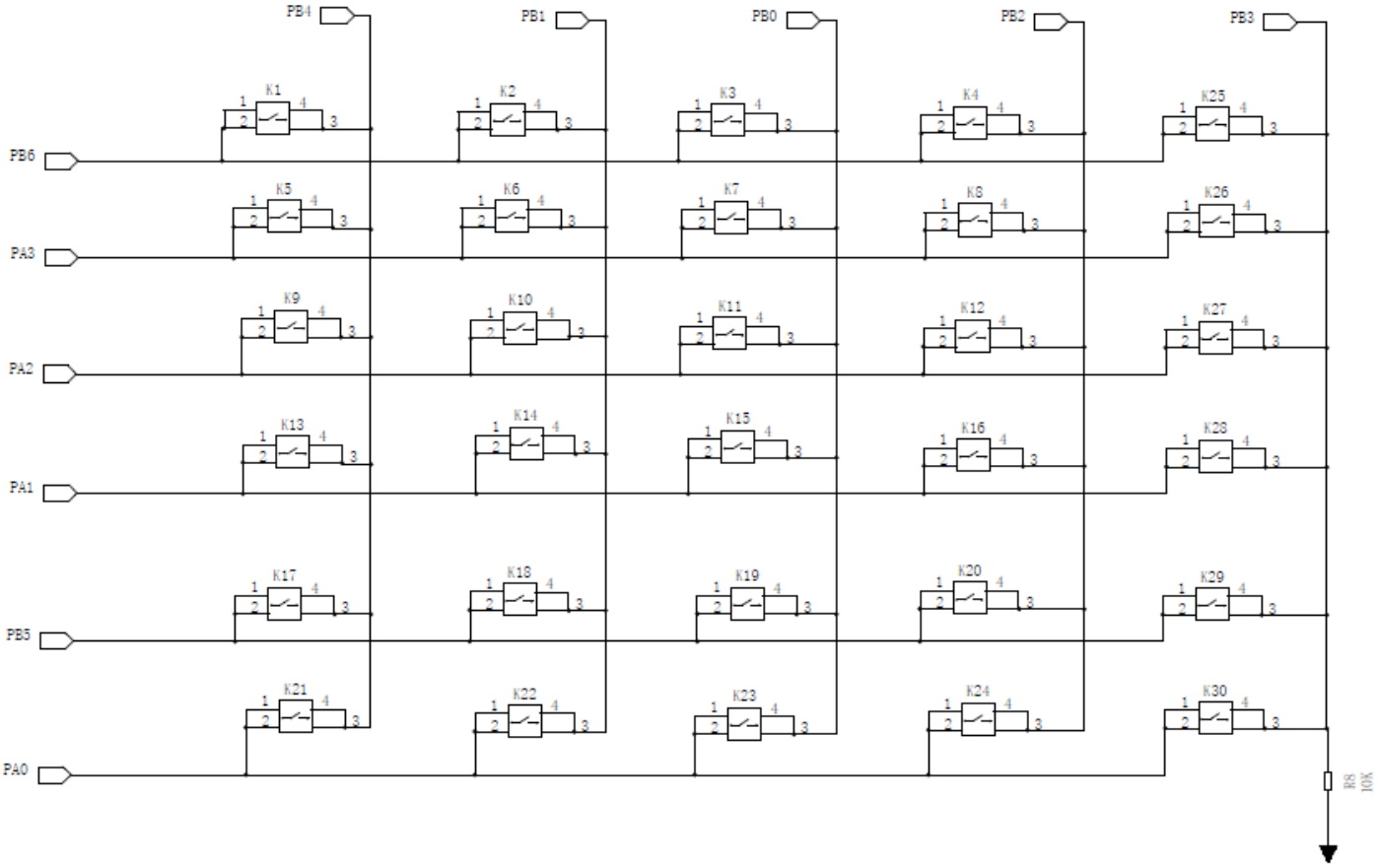
Note: A0 connect to WF306TBM SDIN , B6 connect to WF306TBM SEN , B7 connect to WF306TBM SCLK

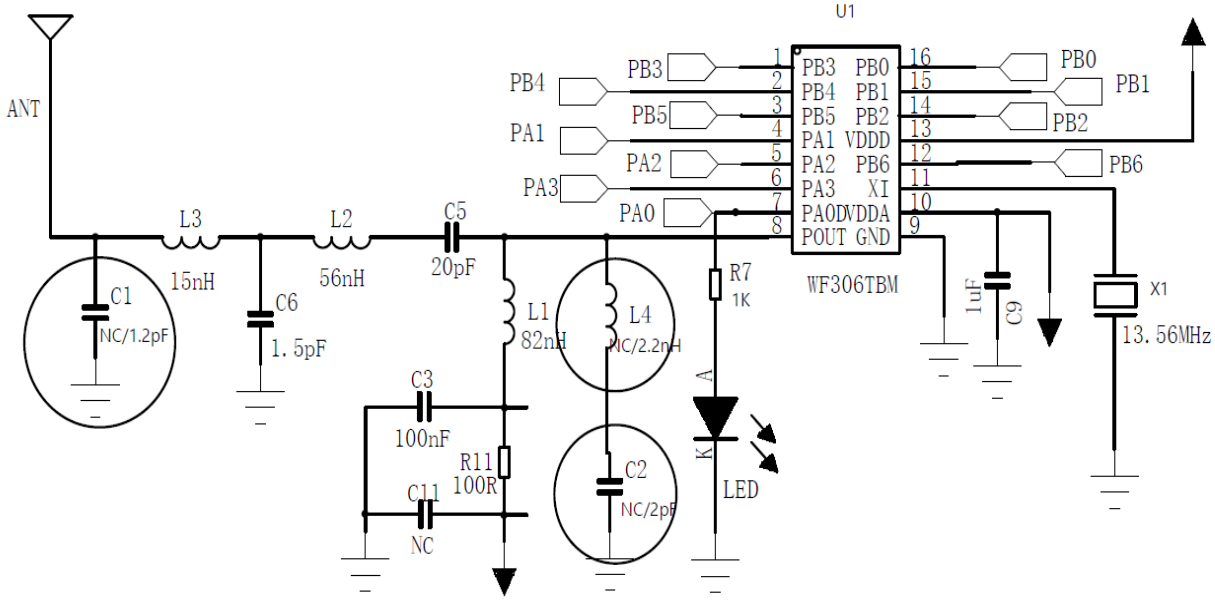
Table 2. Absolute Maximum Rating

Item	Rating
Supply Voltage, VDD	+ 5.6V
Inputs and Clock Outputs	- 0.5V to + 5.6V
Storage Temperature	- 65 to + 150 oC
Soldering Temperature	+ 260 oC

Table 3. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	300MHz-450MHz	2.3	3.0	3.6	V
Supply Current	I_{DD}	Fout=434MHz, 13dBm , 3V		13		mA
RF Power On/Off Ratio	Pratio	300MHz-450MHz		60		dB
Pout supply voltage	Pvol	300MHz-450MHz			3.6	V
Transmitted Power	Pout	Fin=315MHz , Vdd=5V		10		dBm
		Fin=434MHz , Vdd=5V		10		dBm
Data Rate		OOK/ASK mode	0.5		10	Kb/s
OSCI operating Frequency	F_{OSC}		9	10	20	MHz
RC-OSC	Rosc	RC Oscillator		4		MHz
Operating Temperature	T_a		-40	27	85	℃
Leakage Current	I_{SB}	Power down mode			1	uA

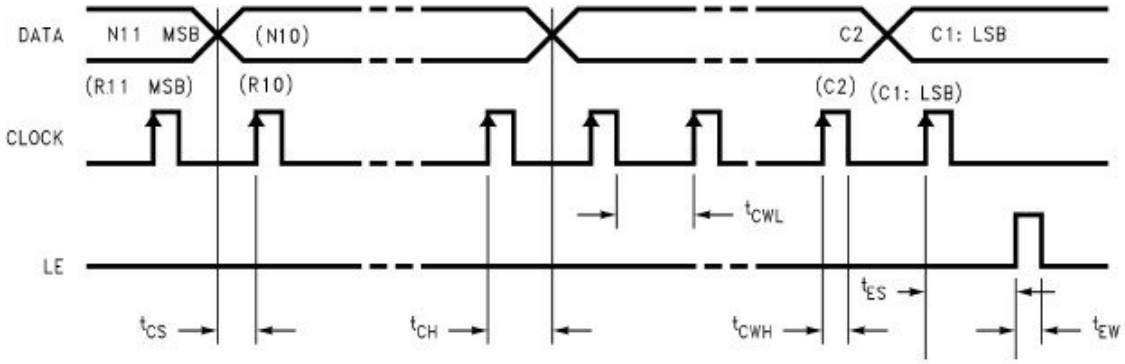

PB4
PB1
PB0
PB2
PB3
PB6
PA3
PA2
PA1
PB5
PA0
K1
K2
K3
K4
K25
K5
K6
K7
K8
K26
K9
K10
K11
K12
K27
K13
K14
K15
K16
K28
K17
K18
K19
K20
K29
K21
K22
K23
K24
K30
R8
10K


U1
ANT
L3
15nH
L2
56nH
C5
20pF
C1
NC/1.2pF
C6
1.5pF
L1
82nH
L4
NC/2.2nH
C3
100nF
R11
100R
C11
NC
C2
NC/2pF
K
A
LED
R7
1K
PB4
PB3
PB5
PA1
PA2
PA3
PA0
PB3 PB0
PB4 PB1
PB5 PB2
PA1 VDDD
PA2 PB6
PA3 XI
PA0DVDDA
POUT GND
WF306TBM
PB0
PB1
PB2
PB6
1uF
C9
X1
13.56MHz

Functional Description

Serial Data input and Timing

WF306TBM has 3-wire interface（CLK, DATA, LE） to set R counter, PLL N counter, and other parameters。At the rising edge of CLK，DATA are written into shift-register (MSB: first input data; LSB: last input data)。At the rising edge of LE, stored data is loaded into mid-latches.



Note: （1） MSB loaded first。

（2） WhenWF 306TBM power is disconnected CLK,DATA, LE are pulled at low

（3）

Symbol	Parameter	Min	Max	Unit
t_{CS}	Data to Clock Setup time	10.5		μs
t_{CH}	Data to Clock Hold time	22		μs
t_{CWH}	Clock Pulse width High	10.5		μs
t_{CWL}	Clock Pulse width Low	20.5		μs
t_{ES}	Clock to LE Setup time	10		μs
t_{EW}	LE pulse width	10		μs

11-Bit data are transfer from shift-register into the latches, MSB first, LSB last. The last two LSB bits control the register address. The bit format is as below.

Where C1, C2 are control bits, determines the register address.

Register Address control bits		Register	Note
C2	C1		
0	0	R0	

0	1	R1	
1	0	R2	
1	1	R3	

For R0 register, R0<8:7> control charge pump current, R0<9> not used.

		R counter						CP current		Not used
LSB										MSB
C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9
0	**0**	R0								

function	R0<8:7>		
	N8	N7	Icp (uA)
	0	0	0.5
	0	1	1.0
	1	0	1.5
	1	1	2.0

R counter is controlled by initial 6-Bits N<6:1>， see below table. Default state, R=10

R<6:1>	N6	N5	N4	N3	N2	N1
1	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
63	1	1	1	1	1	1

Note:

(1) MSB load first。

(2) R≥1

(3) $R = R1x2^0 + R2x2^1 + \ldots + R6x2^5$, R = 1 to 64.

For R1 register, R1<9>=1, power down chip. Other bits control B counter.

		B counter								Global Powerdown
LSB										MSB
C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9
1	**0**	R1								

B counter are controlled through 8-Bits, according to below table, N8 default state is 1, else bits are zeros.

B	N8	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
255	1	1	1	1	1	1	1	1

$B = N1x2^0 + N2x2^1 + \ldots + N8x2^7$, $B \geqslant 1$，Divider ration：1 to 255 ($B \geqslant A$)，

For R2 register, R2<9> not used. R2<8> select N-divider modulus P.

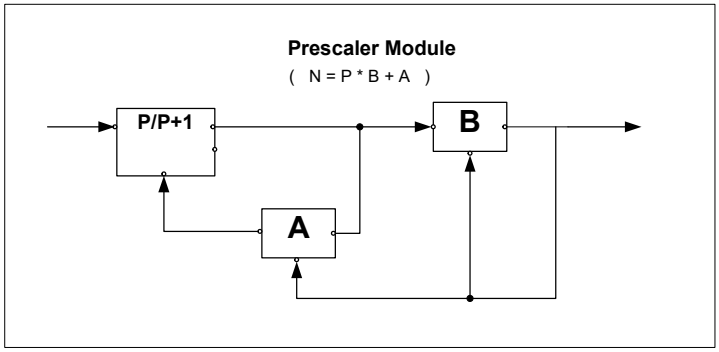
Mode sel	Clk sel	A Counter							N divider select	Spur control
LSB										MSB
C1	C2	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9
1	**1**	R2								

	R2<8> control N-divider mode	
	0	1
function	P=16	P=32

Counter (N) consists of one 7-Bits SWALLOW COUNTER （A Counter), one 8-Bits PULSE COUNTER (B counter)，and one P/（P+1） prescaler。When counter A counts, dual module prescaler divider ration is P+1. When A counter is overflow but B counter still counts, dual module prescaler divider ration is P, P =16, or 32.。While B counter overflow，A counter and B counter both are reset。 Finally the divider ration N is，

$$\mathbf{N = P \times B + A\ ,\ B \geq A}$$

The default state N=320, P=32, B=10, A=0.



A counter is controlled by initial 7-Bits， see below table.

A	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
127	1	1	1	1	1	1	1

Pulse swallow formula： fvco = [(P * B) + A] * fosc / R,

- fvco, VCO oscillation frequency
- B， 11-Bits B counter’s divider ration， 1-255
- A，swallow A counter’s divider ration，0 ≤ A ≤ 127 , A ≤ B.
- fosc, crystal oscillation frequency
- R， 6-Bits R counter divider ration， 1-63
- P， dual module prescaler， P = 16/32.

For R3 register, R3<2:1>=1, not used. R3<6:3> control power amplifier transmitting power. R3<9:7>=1, not used.

		Not used		TX power control				Not used		
LSB										MSB
C1	C2	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9
1	**1**	R3								

R3<6:3>	Function, tune TX power	
0000	Def power	
0001	Max power	
1110	Min Power	

Crystal Oscillator

The crystal oscillator circuit consists of a colpitts oscillator. It can drive 10MHz-30MHz crystal without external capacitors required. The crystal driver stage can also take input clock as input clock buffer.

The R counter is used to divide the crystal clock down to the low frequency clock, which is sent to PFD in PLL block as reference clock.

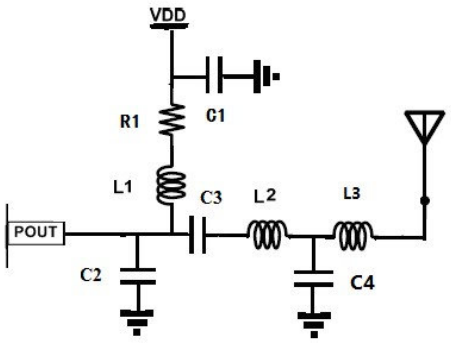
PLL Block

The PLL consists of phase-frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO), and divider (N). The PFD compares two signals and produces an error signal which is proportional to the two signal phase difference. The error signal is used to control the VCO to run fast or slow.

The divider N counter is selectable through SPI interface. The VCO oscillation frequency range is tunable between300MHz-500MHz.

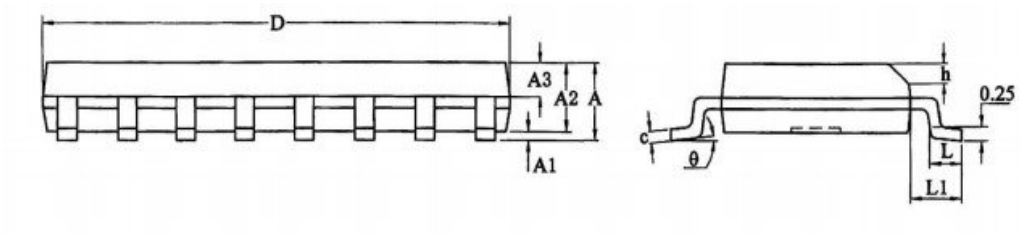
RF OUTPUT

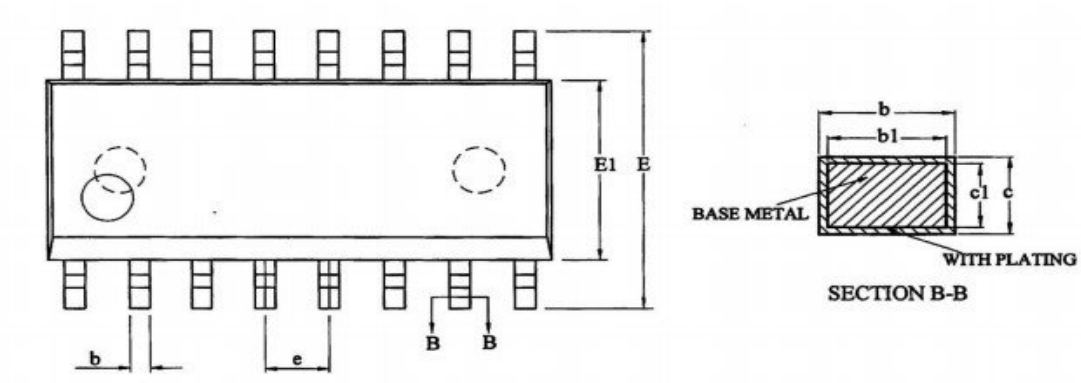
The POUT pin can be matched to 50 Ohm with a T-type circuit. The supply voltage can be as high as 3.6V. Below table is suggested inductor and capacitor value for different frequency.



Frequency (MHz)	L1 (nH)	L2 (nH)	L3 (nH)	C1 (uF)	C2 (pF)	C3 (pF)	C4 (pF)	R1 (Ω)	Note
315	100	82	82	1.0	1.0	5	1.8	100	
433	82	68	68	1.0	1.0	5	1.2	100	

Package Information SOP-16





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°